WHITE RABBIT PTP/IEEE1588

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White Rabbit

SUB-NANOSECOND SYNCHRONIZATION FOR EMBEDDED SYSTEMS

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WHITE RABBIT: SUB-NANOSECOND SYNCHRONIZATION FOR EMBEDDED SYSTEMS

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Abstract

The article describes the design of the White Rabbit PTP Core (WRPC) – an easy-to-use HDL module implementing an IEEE1588-v2 synchronization model extended with the White Rabbit (WR) protocol. The WRPC can provide sub-nanosecond timing in standard FPGA-based designs or enhance the accuracy of existing systems through OEM modules. WRPC delivers the time and frequency reference via a common timing interface (1-PPS, timecode and reference frequency) to simplify the integration with existing modules. It also features a Gigabit Ethernet fiber optic link (1000Base-X) to communicate with other WR-compliant devices.

We also describe the details of the synchronization algorithm of White Rabbit which is implemented in the WRPC. WR combines IEEE1588-v2 timestamping with a synchronous physical layer based on Synchronous Ethernet. Sub-nanosecond accuracy is achieved by actively compensating the link delay using phase measurements done with Digital Dual Mixer Time Difference (DDMTD) phase detectors and on-line calibration of the gigabit transceivers' latencies. The measurements presented in the article show a long-term master-to-slave offset below 1 ns, while the precision is better than 20 ps rms for a 5 km single mode fiber connection.

The protocol is being developed by CERN, Elproma Elektronika, GSI and other institutes and companies. In addition to fine synchronization, it also provides deterministic frame delivery and extended link redundancy features, developed for critical controls applications, such as the control networks of the particle accelerators at CERN

INTRODUCTION

Accurate and precise synchronization in industrial and scientific applications can be provided by many different standards and protocols. These usually are dedicated synchronization systems or custom-made solutions based on time codes, 1-PPS signal and/or reference frequency. They offer very good accuracy/precision, but require dedicated network infrastructure and complex calibration procedures. This in turn increases the cost of the whole application.

Contrary to the dedicated systems, Ethernet-based synchronization protocols allow for coexistence of both timing and regular data in the same network, allowing to build timing systems on top of an already-existing network infrastructure. Unfortunately, the non-determinism of Ethernet results in worse synchronization performance. The active network components: switches, network adapters and OS protocol stacks all add varying, nondeterministic latencies which are difficult to estimate and compensate. As a result, the IEEE1588-2008 (PTP protocol), even with hardware generated timestamps, can achieve accuracies not better than tens of nanoseconds, and only in well-controlled network environments.

The White Rabbit protocol was created at CERN as a successor of the current dedicated timing system for CERN's accelerators. Apart from very accurate synchronization, it also provides the means of deterministic, large-scale monitoring and control of latency-critical accelerator equipment while being scalable and modular. WR combines the accuracy and precision comparable to dedicated timing systems with the real-time performance of industrial networks and flexibility of Ethernet.

One of the hardware modules being developed within the scope of the White Rabbit project is the WR PTP Core (WRPC). It is a standalone HDL module, which can be integrated inside larger FPGA designs or used as a stand-alone plug-in module in already existing devices. The WRPC implements the compact version of the WR PTP protocol and delivers accurate UTC time low-jitter reference frequency via a commonly used timing interface (1-PPS signal, time-code and reference clock).

The first section of this paper describes the synchronization techniques used in WR, which combined together result in sub-nanosecond synchronization accuracy over a 5 km fiber link. The next chapter focuses on the design of the WRPC. The 3rd part presents the measurements that have been performed to prove the WR synchronization quality. Finally, the example applications are shown which could benefit from using WR and WRPC, followed by the conclusions.

WHITE RABBIT SYNCHRONIZATION SCHEME

White Rabbit was developed as an extension to the IEEE1588-2008 (PTP version 2) protocol. The original PTPv2 protocol has serious limitations that prevent from achieving sub-nanosecond precision and accuracy. First of all the resolution of hardware generated timestamps in typical IEEE1588v2 implementations is limited. For example when using a Gigabit Ethernet PHY, the timestamping counter is usually clocked at 125MHz, which corresponds to a theoretical resolution of 8ns (assuming that ingress/egress latencies of the PHY are constant). Secondly, PTPv2 assumes that the underlying networking hardware runs asynchronously, so the syntonization of slave's oscillator is performed by periodically sending *Sync (*or *Sync/Follow_up*) messages. However, in order to precisely compensate the drift of the slave clock, these messages have to be exchanged frequently, generating significant network traffic. Such extra network load may be unacceptable in particle accelerators' applications where there is a strong need of having deterministic network that could deliver critical control messages without any disturbances.

To address those limitations of PTP the White Rabbit protocol combines IEEE1588v2 with Synchronous Ethernet (SyncE), digital phase measurements and calibration techniques described later in this section.

WR LINK DELAY MODEL

To estimate the offset between the two nodes, one must know the accurate one-way transmission delays: master-to-slave $delay_{ms}$ and slave-to-master $delay_{sm}$. The PTP protocol assumes link delay symmetry which means the one-way delays are estimated as exactly the same and equal half of the round-trip delay ($delay_{MM}/2$). In fact this simplification reduces the synchronization accuracy. WR instead considers a few different sources of the link asymmetry and combines them achieving better estimation of the actual one-way delays.

The *WR Link Delay Model* used to calculate the precise master-to-slave delay is presented in Figure 1. In general it can be expressed as the sum of fixed master's transmission circuit delay (Δ_{txm}), variable transmission medium delay (δ_{ms}) and fixed slave's reception circuit delay (Δ_{rxm}):

$$delay_{ms} = \Delta_{txm} + \delta_{ms} + \Delta_{rxs}$$

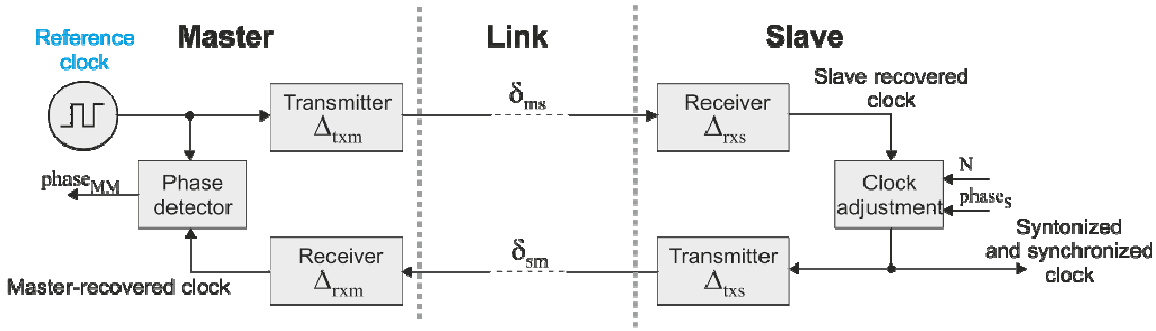

Figure 1: White Rabbit Link Delay Model

Slave-to-master delays can be expressed analogously with Δ_{txs}, δ_{sm} and Δ_{rxm}. These delays can be then split into two groups: values constant for a given connection ($\Delta_{txm,rxm,txs,rxs}$) and values that can vary during the link's operation ($\delta_{ms,sm}$). The fixed values are measured when the connection is being established (during the *PHY calibration* process). WR currently uses a single, wavelength-multiplexed (WDM) fiber for two-way communication to simplify the estimation of link asymmetry. Knowing that length of the fiber is exactly the same in both directions, the delay asymmetry is directly and solely caused by the difference in wave propagation velocity. Taking for example $\lambda_{tx} = 1550nm$ and $\lambda_{rx} = 1310nm$ the *relative delay coefficient* is introduced and defined as:

$$\alpha = \frac{\delta_{ms}}{\delta_{sm}} - 1 = \frac{n_{1550}}{n_{1310}} - 1$$

where n_{1550}, n_{1310} are the refractive indexes. However, the refractive indexes may slightly differ between different fiber manufacturers. Therefore, for applications demanding very high accuracy or using long fibers, the α parameter can be determined in laboratory, from on the value of $delay_{MM}$ (performed by the PTP software) and the master-slave skew (measured with an oscilloscope). Finally, having the α coefficient the accurate one-way delay is computed using the following relations:

$$\Delta = \Delta_{txm} + \Delta_{rxs} + \Delta_{txs} + \Delta_{rxm}$$

$$delay_{MM} = \Delta + \delta_{ms} + \delta_{sm}$$

$$delay_{ms} = \frac{1+\alpha}{2+\alpha}(delay_{MM} - \Delta)$$

After computing the accurate one-way delays, one can calculate the offset between master and slave clocks and use it to compensate the clock skew:

$$offset = t_2 - t_1 + delay_{ms}$$

SYNCHRONOUS ETHERNET

Ethernet physical layer can be used to transfer frequency traceable to an external precise source (e.g. a cesium clock or a GPSDO). Synchronous Ethernet (Sync-E) does this in the same way as in SONET/SDH. Those in turn have already proven the ability of transmitting precise timing over long distances. The performance of syntonization provided by Sync-E does not depend on the momentary network load and it is not severely affected by increasing length of the link. Clock recovery is implemented in the hardware, using a Clock-Data recovery type of a PLL, independently from the modules participating in packet transmission/reception.

In fact, such syntonization mechanism exists in all Ethernet PHYs, but the recovered clock is only used to sample the incoming data, whereas the transmit path is timed by the device's free running local oscillator. On the other hand, every SyncE node in the network takes the recovered clock from the layer closer to the timing master and locks its LO to it. This way, the whole network has a common notion of frequency, as shown in Figure 2.

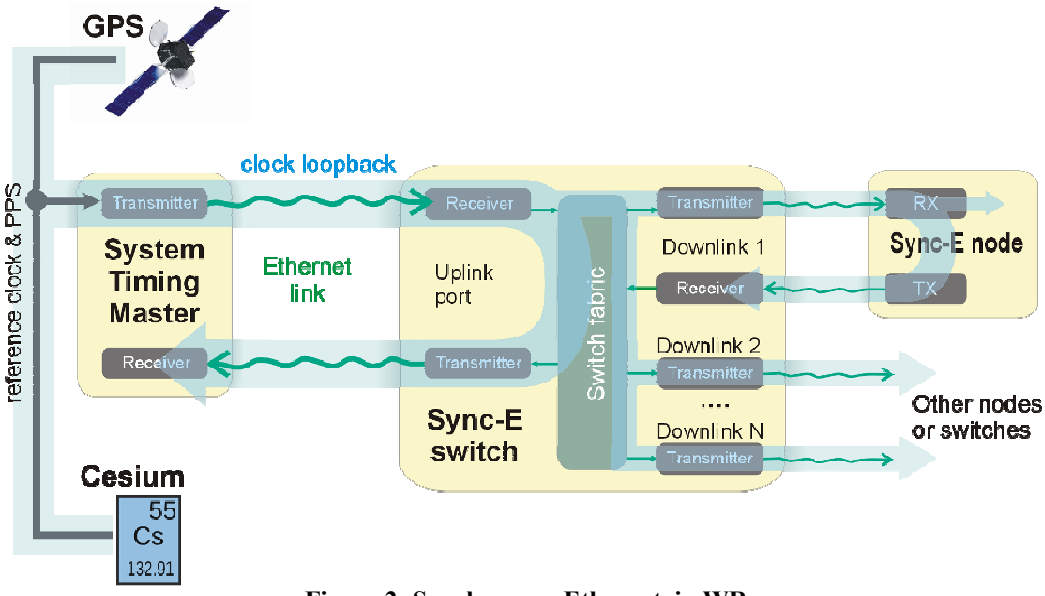

Figure 2: Synchronous Ethernet in WR

White Rabbit is a hierarchical network structure with a System Timing Master(s) (STM) on the top. Multiple timing masters can be used as redundant reference sources, provided that they are externally synchronized with each other at a sub-nanosecond level. With the frequency transfer done on the hardware layer, the role of the PTP is reduced just to measuring and compensating the link delay and clock offset. Moreover, synchronous network operation allows for casting accurate time measurements into phase shift measurements which offer better precision and accuracy while lowering the complexity of the hardware.

DIGITAL DMTD PHASE DETECTOR

Once the slave's oscillator is syntonized with the master clock signal, a phase detector technique is used to measure the round-trip link delay with sub-nanosecond accuracy by employing a Digital Dual Mixer Time Difference (DDMTD) phase detector. Aside from producing accurate packets' timestamps, DDMTDs are also used to determine the Tx/Rx PHY latencies during the PHY calibration process.

Direct measurement of phase shift between two Ethernet clock signals (using a gated counter) is not a simple task, since the counter would have to operate at a much bigger frequency than the measured signals (125 MHz). One of the methods of tackling this problem is moving the frequencies of the measured signals and preserving their phase relationship into a low bandwidth baseband, where the phase measurement can be easily done with a counter. An example of such analog Dual Mixer Time Difference (DMTD) system is presented in Figure 3. The input to the DMTD detector are two signals under consideration *a(t)*, *b(t)* which have the same frequency and amplitudes, but different phases. Additionally the local oscillator having the frequency (f_{offset}) close to the reference (f_{clk}) is needed. Two mixers multiply measured cosine signals with the local oscillator resulting in the following formula:

$$a(t) \bullet c(t) = \cos(2\pi t f_{clk} + \phi_a) \bullet \cos(2\pi t f_{offset} + \phi_{offset})$$

$$= \frac{1}{2}\cos[2\pi t(f_{clk} + f_{offset}) + \phi_s + \phi_{offset}]$$

$$+ \frac{1}{2}\cos[2\pi t(f_{clk} - f_{offset}) + \phi_a - \phi_{offset}]$$

The product is the sum of two signals, but the one having higher frequency is filtered out with low-pass filters. The downconversion process changes the frequency but leaves the phase difference unchanged. For example $f_{clk} = 125MHz$ and $f_{offset} = 124.99MHz$ will produce a 10 kHz output signal. The phase shift between *a(t)* and *b(t)* after such transformation can be easily measured using a simple counter.

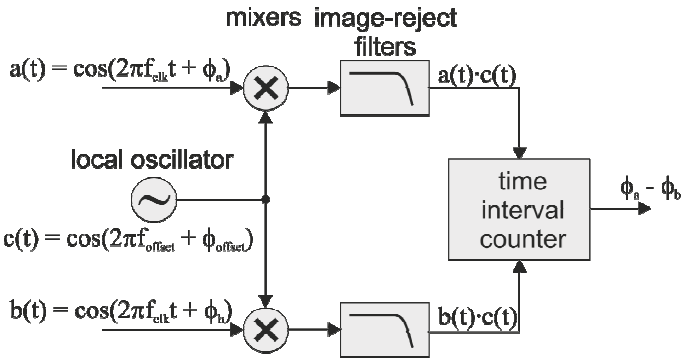

Figure 3: Analog DMTD

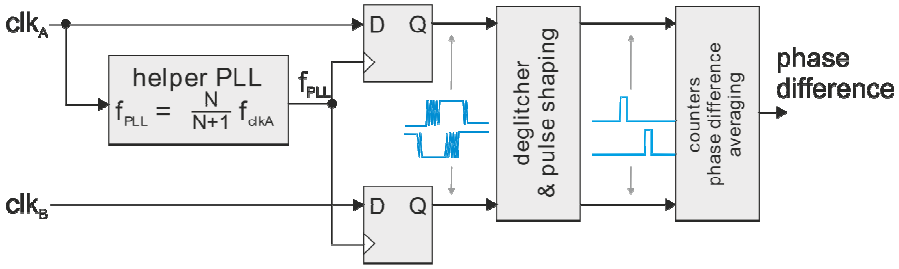

Figure 4: Digital DMTD

While analog DMTDs provide exceptional resolution and linearity, they require complex and relatively expensive external discrete components (mixers, filters). The cost issue becomes particularly important in multi-port devices, such as the White Rabbit switch, which have to perform phase tracking simultaneously at all the ports. Therefore, a digital counterpart of a classical DMTD system was developed at CERN. Figure 4 presents the structure of a Digital DMTD (DDMTD), where analog mixing is replaced with digital sampling operation.

A DDMTD uses D-type flip-flops instead of mixers (which can be considered as being one-bit analog-to-digital converters) and measures phase shift between two square wave clock signals clk_A and clk_B. Locking the offset frequency to the frequency of one of the input signals ensures that the period of waveform at the output of the flip-flops is constant, simplifying the calculation of the phase shifts (no division required) and making the resolution and linearity independent of the stability of the offset oscillator. The only external component used in the presented method is a voltage-controlled crystal oscillator, generating the offset clock (*helper PLL* block in Figure 4), the remaining logic is implemented entirely within an FPGA.

Thanks to the very small hardware footprint of a DDMTD detector, multiple DDMTDs can be parallelized to increase the resolution by averaging measurement results from multiple sub-detectors connected to the same input signals. A DDMTD detector can be also used within a PLL, forming a very linear phase shifter with acceptable level of added jitter. The WR Core uses such phase shifter to align the phase of the slave clock with the master clock.

PHY CALIBRATION

The transmit (TX) and receive (RX) latencies of a Gigabit Ethernet PHY ($\Delta_{txm,rxm,txs,rxs}$) can be different each time the device is powered up or the link is established. There exist PHYs that provide these latencies directly for the user's HDL core (Altera Stratix/Arria FPGAs) and some other vendors (Xilinx GTP/GTX) allow for FPGA-internal calibration of TX/RX latency (using a *bit-slip* method)**.** In order to stay hardware-agnostic, the latencies in WR can be measured during the *PHY calibration* process each time the connection between nodes is established (Figure 5). Those latencies in most PHYs remain constant while the Phase-Locked Loop/Clock Data Recovery is locked.

The Tx latency is measured by feeding the transmit path with a sequence of K28.7 8b10b characters (*1111100000*). These symbols effectively create a 125MHz square wave on the serial outputs of the transceiver, so the TX latency can be measured with a DDMTD as the phase difference between the PHY's TX clock input and its serial output. The RX path is calibrated in an identical way, except that the K28.7 calibration pattern is produced by the PHY on the other end of the link.

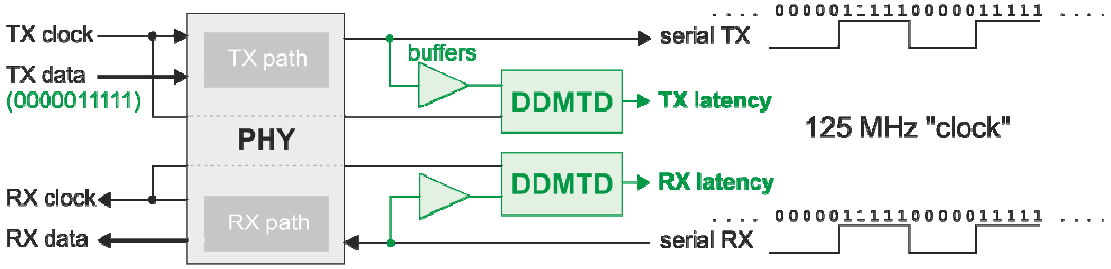

Figure 5: Ethernet PHY calibration using DDMTD detectors

WR EXTENSION TO PTP

As mentioned in the introduction, White Rabbit employs PTP to measure the varying link delay, as well as to schedule the PHY calibration and syntonization hardware processes. Since IEEE1588v2 provides very convenient customization facilities (such as profiles, and Type-Length-Value packet fields), White Rabbit 's sub-nanosecond extensions (further abbreviated as WRPTP) were introduced without breaking the compatibility with the original PTPv2 standard.

One of the extensions in WRPTP is the *WR Link Setup*. It is the packet exchange process where two nodes try to establish a WR link. It encompasses the identification whether the node is WR-compliant, the syntonization, and the measurement of the WR-specific parameters. These values are exchanged over the network and used for further precise delay and offset calculations. During the *WR Link Setup* process , PTP messages with custom TLV fields are sent, and a separate state machine (*WR State Machine*) is executed. The diagram in Figure 6 presents the transitions in the *WR State Machine* (*WR FSM*) and the packets being exchanged. The *WR FSM* is executed when the main PTP state machine is in *PTP_UNCALIBRATED* state (slave nodes) or in *PTP_MASTER* state (master nodes).

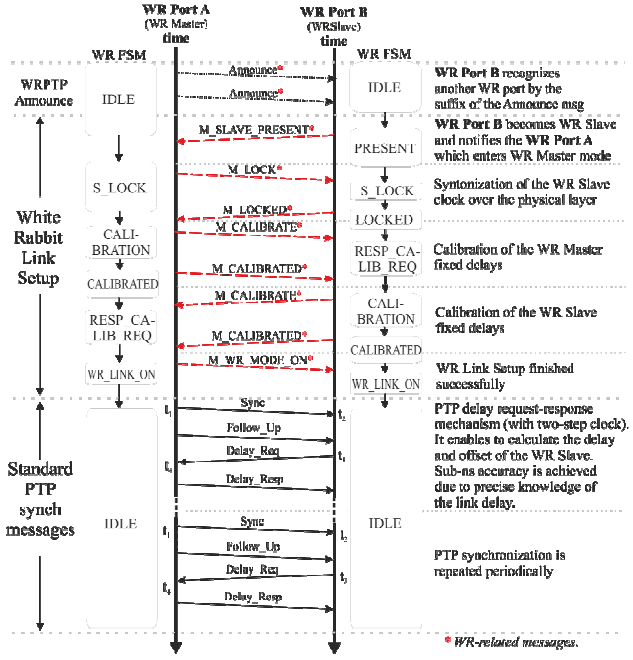

Figure 6: White Rabbit PTP extension

At the beginning the WR Master sends periodically the *WR Announce* messages, which indicate that the master node is WR-compliant. The WR Slave responds with the *M_SLAVE_PRESENT* message, while standard PTP slaves ignore the message (and so the master initiates a standard PTP session). The first step of establishing a WR link is the syntonization. The WR Master requires the slave to start this process by sending *M_LOCK message*. In this stage, the 125MHz clock signal recovered from the incoming data stream becomes the reference for the local PLLs via *SyncE*. As soon as the PLL is locked, the slave node responds with *M_LOCKED*. This starts the calibration process. After receiving *M_CALIBRATE* WR Slave generates the calibration pattern of requested duration, so that the master can measure its PHY's RX delay. This lasts until the master issues *M_CALIBRATED* message and is followed by the WR Slave calibration, done in an analogous way. Finally, the master finishes the *WR Link Setup* by sending *M_WR_MODE_ON* and the PTP daemon commences its regular operation according to the PTP State Machine. During that, the WR link model is taken into account to improve the accuracy of one-way delay and master-to-slave offset calculations.

WHITE RABBIT PTP CORE

The implementation of the WR-PTP protocol and appropriate network hardware is not a trivial task. The White Rabbit PTP Core (WRPC) was created to simplify the integration of the WR into both existing and arising embedded devices and systems. It is an HDL module that could be easily synthesized and used as a standalone WR interface inside a single FPGA chip or as an IP core in a larger design. WRPC implements an IEEE1588 ordinary clock capable of reaching sub-nanosecond accuracies and working both in Master and Slave modes. In master mode the WRPC uses externally-provided reference time and frequency to synchronize other WR compliant devices. When running in the slave mode, WRPC receives the timing information from a PTP master, synchronizes its internal clock and provides the timing information for other IP cores through a simple VHDL interface.

The WRPC has a single Gigabit Ethernet interface, currently supporting 1000Base-X optical Ethernet (1000Base-T copper support in development). Inside, it hosts a custom-designed Ethernet MAC and a 32-bit RISC CPU surrounded by additional modules required to implement the WRPTP protocol. The WRPC as a black-box is shown in Figure 7. The only necessary external components are two digitally tunable 125MHz oscillators (one for the main PLL, and one for producing the DDMTD offset frequency). The remaining blocks outside the WRPC are optional and their use depends on the particular application. An optional I^2C interface is provided for attaching an external EEPROM, which can store the device's configuration data (MAC address and calibration parameters). WRPC has been successfully tested with GTP and GTX transceivers integrated inside Xilinx's FPGAs as well as generic Ten-Bit Interface (TBI) PHYs[1]. Support for Altera GX PHYs is currently being implemented.

[1] Teras Instruments TLK1221

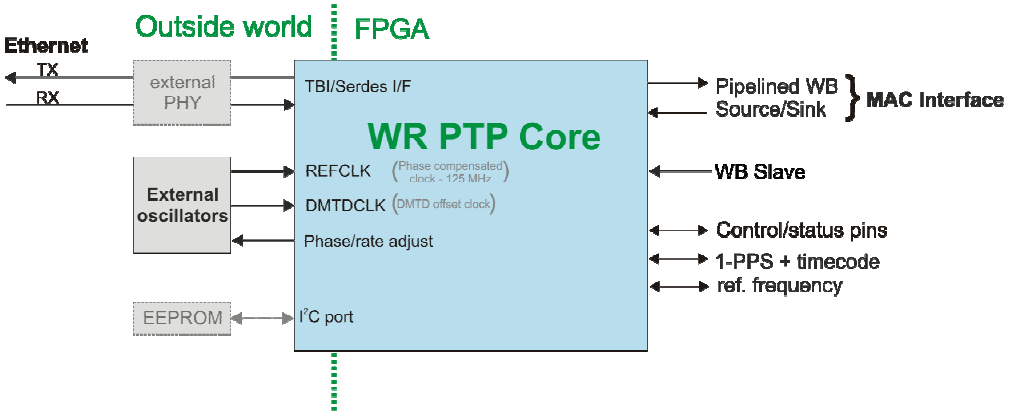

Figure 7: White Rabbit PTP Core with possible interfaces

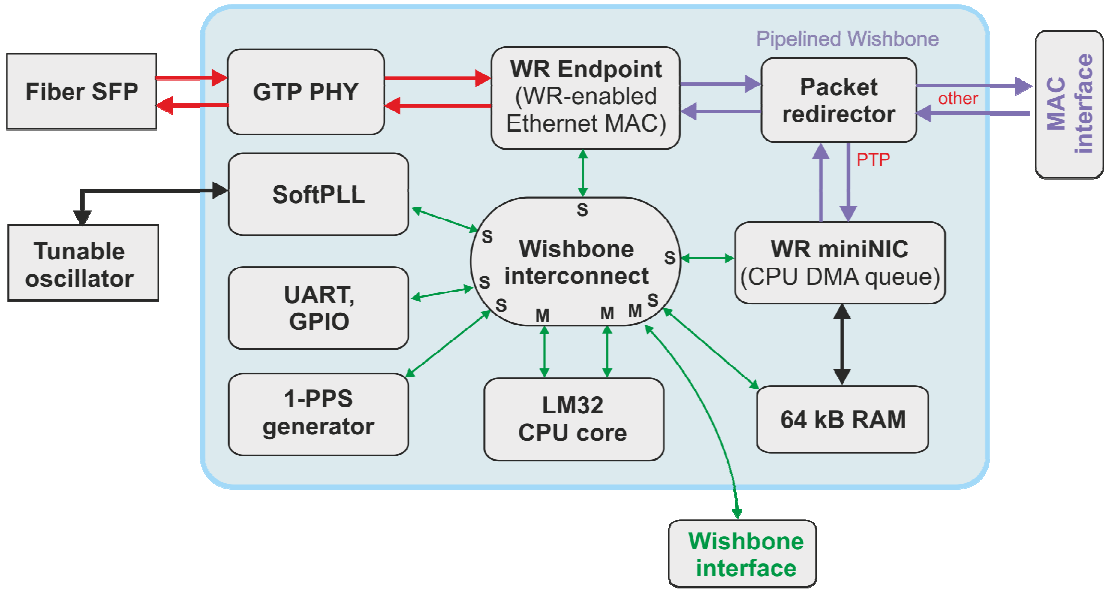

Figure 8: Internal modules of WRPC

The WRPC interfaces with the rest of the system through the following interfaces:

- **Timing port**, incorporating 1-PPS, timecode (UTC and nanoseconds counters) and the reference frequency (125MHz) signals. Depending on the mode of operation (master/slave), timing port either server as an input for an external reference or outputs the recovered synchronized signals. The WRPC can also discipline an auxiliary 125 MHz tunable oscillator.
- **Ethernet MAC interface**, passing non-PTP Ethernet traffic between the integrated Ethernet MAC (WR Endpoint) and the user application. The MAC interface is based on the well established, open Wishbone interface, operating in *pipelined* mode (Figure 8). The *Packet redirector* block inside the WRPC distinguishes between non-PTP and PTP packets and redirects the former to the external MAC interface and the latter to the CPU packet queue. Additionally, the redirector can be programmed to classify the incoming packets according to a set of user-defined rules, relieving the designer from implementing an external packet filter. WRPC MAC interface is also capable of providing cycle-accurate Tx/Rx timestamps for every incoming/outgoing packet for the user application.

- **Wishbone slave** port for accessing the internal control registers, debugging or loading the embedded CPU firmware.

The heart of the White Rabbit PTP Core is the LatticeMico32 (LM32) soft-processor. It is a Harvard architecture, 32-bit CPU optimized for FPGAs, designed by Lattice Semiconductor. The Verilog source code of the soft-core is open and there are no restrictions regarding implementations on FPGAs made by other vendors. The system bus is based on the *pipelined* Wishbone standard, with the CPU and the peripherals connected to a shared crossbar interconnect. The CPU runs a compact version of the WR-PTP software stack, which is stored in 64 kB of the integrated RAM. The PTP daemon is running in a freestanding mode, without any operating system. The PTP-related network traffic is written and read directly from the RAM via the Mini Network Interface Card (*miniNIC*), which implements a simple DMA engine.

The phase measurements and offset compensation is performed by a dedicated digital PLL core (SoftPLL). The SoftPLL instantiates the DDMTD detectors for the phase shifting Main PLL and a frequency detector for the Helper PLL (producing the DDMTD offset frequency). The actual PLL control algorithm is implemented in software and utilizes the vast processing power of a 32-bit modern CPU, resulting in a significant reduction in the FPGA resource footprint.

PERFORMANCE MEASUREMENTS

In order to evaluate the accuracy and precision of synchronization provided by the WR PTP Core, a test system depicted in Figure 9 was built.

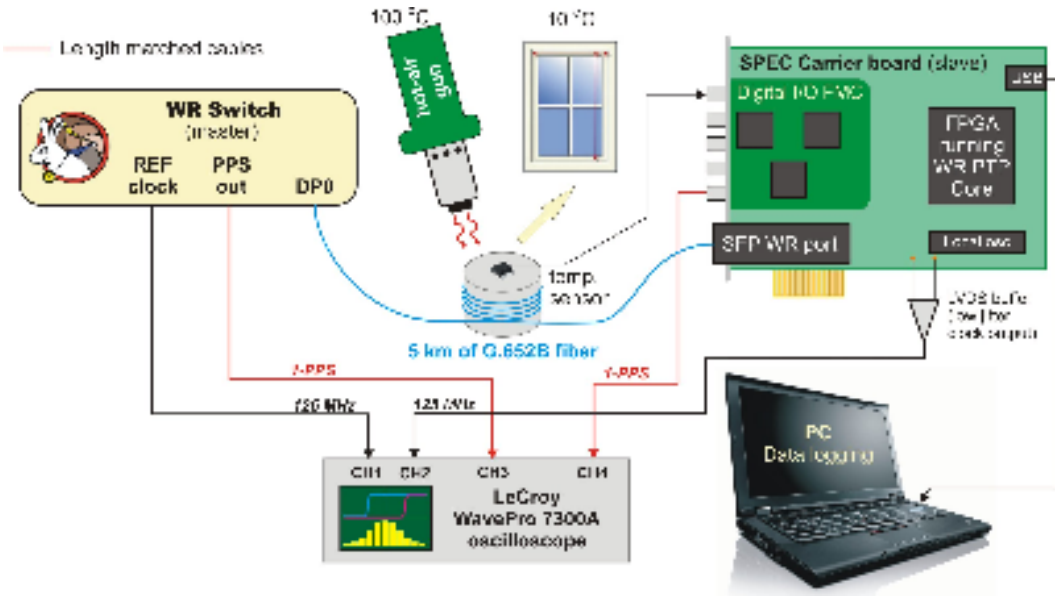

Figure 9: WRPC test system

The system consisted of a WR Master node (a WR Ethernet switch) and a WR Slave node (the WRPC), connected together with a 5 km single mode fiber link. The link used bidirectional (WDM) SFP transceivers operating at wavelengths of 1310/1550 nm. The WRPC was running on a SPEC board (Simple PCI Express Carrier), which is the WRPC's reference development platform. The core was implemented in a Xilinx's Spartan-6 XC6SLX45T FPGA and used a Xilinx GTP transceiver as the physical network interface.

Varying link delay was forced by repeatedly heating up the fiber roll with a hot-air gun and cooling it down by placing outside the window. The temperature of the fiber was continuously monitored by a digital temperature sensor connected to the SPEC board. The relation between the fiber temperature and the round-trip delay is shown in Figure 10.

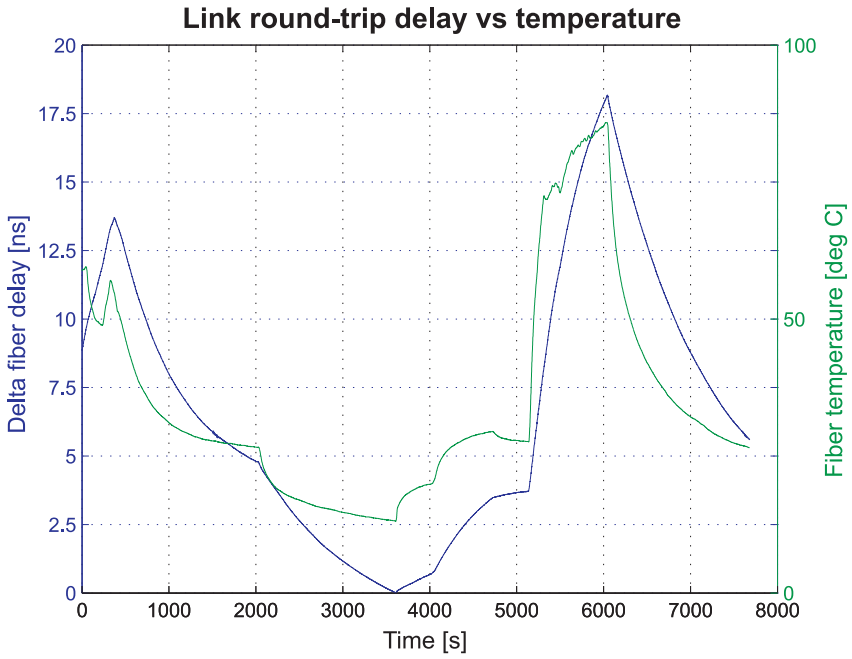

Figure 10: Temperature-induced changes in the round-trip link delay

The measurement lasted for 2.5 hours and the link was tested at temperatures from +12.5 ^{O}C to 85 ^{O}C. The resulting temperature-induced delay drift, measured by the WRPC, was of 17.5 ns. Stability of synchronization was characterized using a high speed digital oscilloscope (LeCroy WavePro 7300A), which was measuring the offset between the 125 MHz reference clock at the master side, and the recovered 125 MHz clock on the slave side. The results are presented in Figure 11.

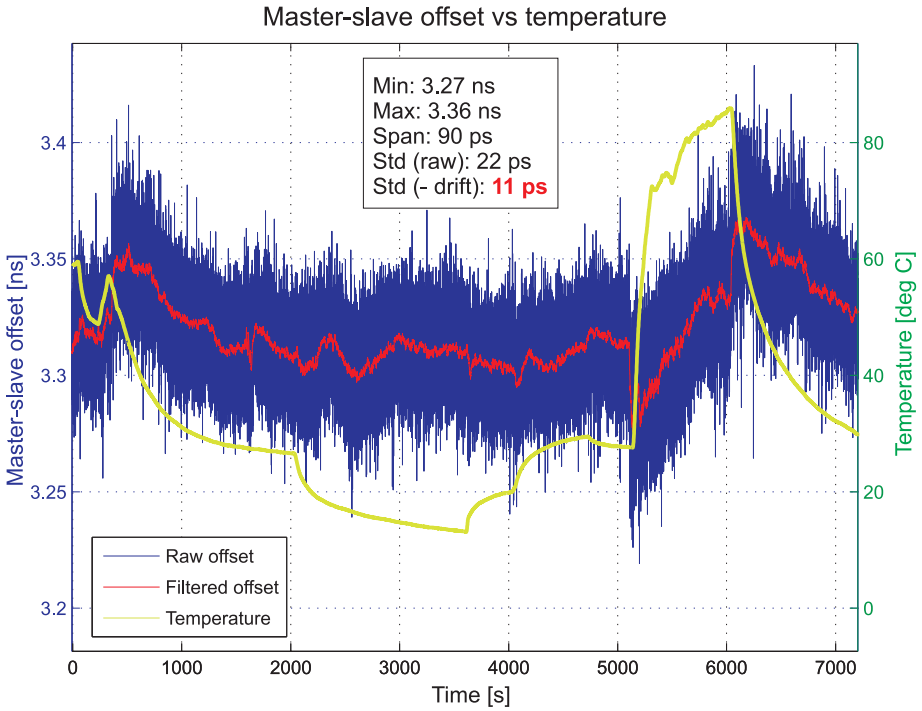

Figure 11: Master-slave 125 MHz clock offset vs fiber temperature

The measured drift was below 100 ps over the entire temperature range (< 1 % of the change in the round-trip delay), while the short-term (< 1 minute) rms master-to-slave jitter was smaller than 11 ps. The noticeable correlation between the offset value (red trace) and the temperature (green trace) was caused by the instability of the transmit wavelengths of the SFP transceivers and can be further improved by stabilizing the temperature of the lasers. The 3.3 ns constant bias results from unmatched cable lengths used to connect the SPEC card and the WR Switch to the oscilloscope (the SPEC does not have a dedicated 125 MHz output, therefore an external LVDS to LVTTL buffer was soldered to the circuit board, introducing a constant 3.3 ns offset).

The presented measurement system was also used to characterize the accuracy of synchronization, by monitoring the offset between the 1-PPS outputs of the master and the slave node. The resulting PPS offset histogram is presented in Figure 12. Note that the jitter is much higher compared to the 125 MHz reference clock offset measurement, since the PPS outputs were driven by the FPGA output pins.

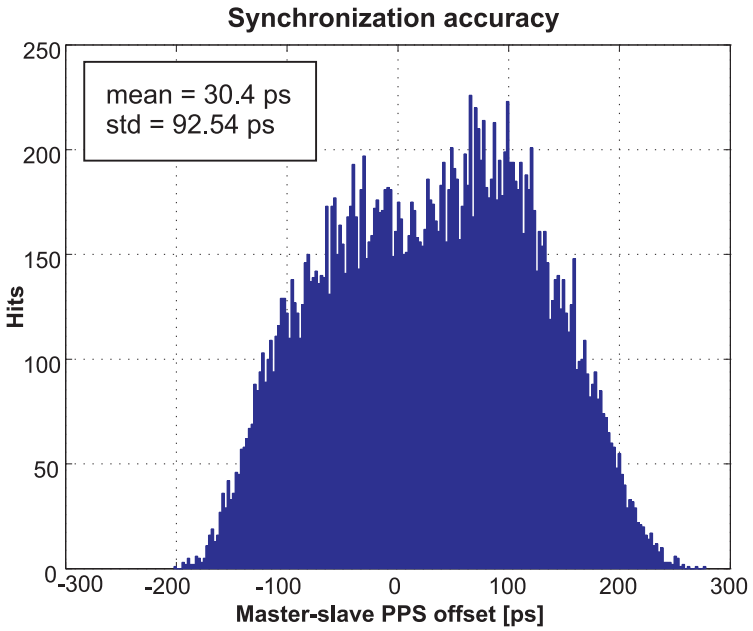

Figure 12: 2.5 hour master-slave PPS offset histogram

APPLICATIONS

Although the initial aim of the White Rabbit project was to meet the requirements of the timing distribution at CERN, its ability to achieve sub-nanosecond synchronization can also be used in scientific projects and to increase the performance of commercial systems and applications.

One field of applications of WR are distributed data acquisition systems, for example the *OASIS* system at CERN, which acts as a huge oscilloscope measuring thousands of signals coming from sources distant by several kilometers. WR can be used to accurately time tag the blocks of samples at the ADC cards and produce nanosecond-accurate time tags for the external trigger signals. Having the sample blocks with associated time tags, one can reconstruct the original time relations between the signals and the triggers in software and present the measurements to the operator as if it was displayed on a typical oscilloscope.

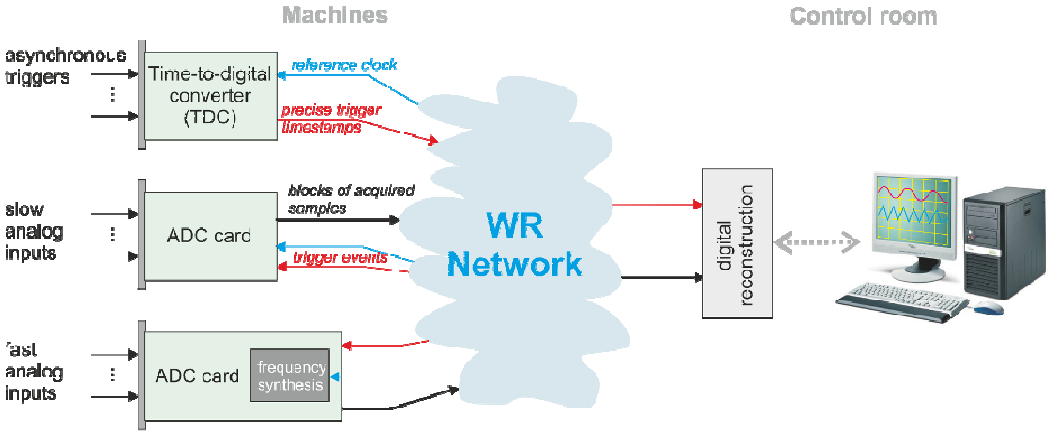

Figure 13: Distributed oscilloscope using WR network

The WRPC module and the WR protocol could be also used in commercial systems and applications. The radars, terrestrial precise approach instrumentation in airports and next generation mobile telecommunication networks are the flagship examples of systems requiring very precise timing. Currently we are at a time when providers try to fulfill the growing need for high bandwidth and reduce the maintenance costs at the same time. The Long Term Evolution(LTE) and LTE-Advanced[2] define an all-IP network architecture where all traffic (both data and voice) is being transmitted using IP packets. That is why the synchronization standards used before (SONET/SDH) can no longer be used. IEEE1588-2008 was proposed as an alternative, however the LTE-Advanced in a few years would bring up new services and solutions further increasing the amount of transmitted data and requiring even more precise timing that IEEE1588-2008 could not achieve. Two examples of such upcoming technologies are Multi-Cell MIMO and Multi Broadcast Multimedia Services (MBMS). The former would significantly increase the throughput especially at the cells boundary. Mobile device would have multiple antennas (eight is proposed) to be able to receive data simultaneously from multiple base stations. The other technology (MBMS) is being developed for multimedia streaming (mobile TV). This would also rely on simultaneously receiving data from multiple base stations. In both situations the devices forming the LTE-Advanced network would have to be very precisely synchronized. This could be fulfilled by using the WRPC module described in this paper. By using SyncE and phase detection techniques, White Rabbit transmits frequency, precise time and compensates the link imperfections, while introducing negligible amount of additional traffic. The huge advantage of WR in this application is that it is still backwards compatible with IEEE-1588. This in turn means that PTP-compatible devices deployed for handling LTE could be also synchronized from the WR network, and become gradually upgraded in the future to the new LTE-Advanced equipment.

CONCLUSION

White Rabbit proves that sub-nanosecond accuracies are achievable in low-cost, Ethernet based networks. However, WR is not only an advanced synchronization system, exceeding the limits of existing technologies. It is also a prominent Open Hardware and Open Software effort and an example of successful collaboration between the scientific community (CERN, GSI) and the industry (Elproma Elektronika, Seven Solutions and others).

The synchronization protocol and the WR-compliant hardware have been deliberately built on top of open and well established standards with no restrictive licensing, to ensure its portability, facilitate adoption on different hardware and software platforms and cover multiple fields of applications.

The extensions to IEEE1588v2 developed for White Rabbit provide excellent synchronization accuracy at lower message exchange rate, but also ensure that WR-compatible devices interoperate with standard PTP gear. There is an ongoing effort of fully standardizing WR as an official IEEE1588 profile.

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